over Maikihara et al. (US Pat. No.5,243,573) in view of *Garcia* (US Pat. No. 5,949,259). Applicant respectfully traverses the rejections. Favorable reconsideration is requested.

Applicant reiterates the arguments set forth in the response of August 22, 2002. Regarding the rejections under 35 U.S.C. §112, paragraph two, Applicant submits that the pending claims particularly point out and distinctly claim the subject matter of the invention. Lines 17-20, page 11, which were cited by the Examiner, correctly point out that the clock skew reducing circuit accomplishes a reduction in skew, and not the input buffers. However, it is not entirely understood why this section of the specification was cited in the first place. None of the rejected claims recite the input buffers as performing a skew-reduction function.

The Examiner also cited the limitation "the first and second inverters function to reduce the skew present in the complementary clock input signal" recited in claim 1 as being misdescriptive. However, these inverters are disclosed in the specification (see first paragraph, page 12) as part of the clock skew reducing circuit. Thus, it is not understood how this limitation was interpreted as misdescriptive. Should the rejection be maintained, Applicant kindly asks the Examiner to expound on how this limitation is misdescriptive and/or ambiguous.

Similarly, it is not understood why the Examiner cited claims 82 and 91 as being incomplete because there "is no recitation of element to provide method/step to reduce skew." (office action, page 2, last paragraph). Both claims conspicuously recite the method of "modifying the transition of one of said external clock signals relative to the other to produce, from said external clock signals, internal clock signals, which have

reduced skew." This is a method claim which does not require a structural element. Again, should the rejection be maintained, Applicant kindly asks the Examiner to expound on how this limitation is "incomplete."

Accordingly, Applicant respectfully submits that the rejections under 35 USC §112, second paragraph are improper and should be withdrawn.

Regarding the *Makihara* reference, and its application to the §102 and §103 rejections, the Applicant repeats that *Makihara* does not teach or suggest all the features of the presently claimed invention, and particularly the skewed complementary clock signals, and reduced skew output, recited in independent claims 1, 16, 26, 82, and 91.

The Examiner has repeatedly and erroneously asserted that the circuit in *Makihara* receives and outputs complementary clock signals. Again, Applicant points out that nowhere in *Makihara* is there even mention of a "clock signal." A clock signal is generally defined as one that "supplies timing pulses to pace the operation of [a] system" (Gibilisco, S., *The Illustrated Dictionary of Electronics*, 8th ed., p. 119 (2001)). The specification in the present invention defines clock signals consistently with this definition as "signals that vary between a low voltage and a high voltage at regular intervals and are referenced to a fixed voltage, typically either the low voltage or the high voltage" (specification, page 1, lines 9-12).

The teaching in *Makihara*, however, is quite clear that the transistor configuration 24-27 is used to effect amplification of the sense amplifier activating signal (SE) until the difference between the voltage at nodes N4 and N5 is substantially equal to

the source voltage level and the ground level (col. 4, lines 29-30, 54-61; col. 6, lines 21-32). This application has nothing to do with the processing of clock signals.

The Examiner also argued that, since the inverters in *Makihara* are in anti-parallel, their input/output signals are complementary (Office Action, page 3 and 6). However, this interpretation neglects the inputs and connections received at each inverter stage. Claims 1, 16 and 26 recite, among other things, the first and second inverters as *receiving* first and second complementary clock signal input lines. In *Makihara*, no such complementary lines are disclosed.

Also, while the Examiner claims issues of inherency under MPEP 2112, Applicant submits that no rationale or evidence has been submitted to show this inherency as required by MPEP 2112. "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic *necessarily* flows from the teachings of the applied prior art." *Ex Parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990); MPEP 2112. "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999); MPEP 2112. Since *Makihara* fails to disclose complementary clock signals, and further fails to address clock skew, Applicant submits that the reliance on inherency is improper.

Accordingly, Applicant respectfully submits that the rejections under 35 USC §102 as to claims 1-7, 16-19, 82 and 86-90 are improper and should be withdrawn.

Regarding the teachings in *Garcia*, there is nothing in the disclosure that teaches or suggests the input of complementary *clock* signals, nor is there any disclosure of reducing skew rates within the clock signals. *Garcia* does not cure the deficiencies of *Makihara*. Accordingly, the rejections as to claims 8, 11-13, 20, 23-33, 36-37, 83-85 and 91-98 are also improper and should be withdrawn.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejections of the claims and to pass this application to issue.

Dated: February 4, 2003

Respectfully submitted,

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